IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Appln. No. :	10/707,841	Examiner: Chen, Jack S.J.
Filed :	January 16, 2004	Confirmation No.: 1840
For :	METHOD AND STRUCTURE FOR CONTROLLING STRESS IN A TRANSISTOR CHANNEL	

Commissioner for Patents
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RESPONSE TO NOTICE OF NON-RESPONSIVE REPLY

Sir:

In response to the Office Action dated January 6, 2006, Applicants repeat the election of Group I, claims 1-17 and Species I, figures 2A-2L, without traverse. Applicants submit that claims 1-17 read on Species I for the reasons set forth in the Remarks section below.

In the event that the Examiner does not agree that claims 1-17 read on Species I and does not withdraw the Notice of Non-Responsive Reply, Applicants provisionally elect claim 31, with traverse. Applicants submit that claim 31 reads on Species I for the reasons set forth in the Remarks section.

A listing of claims is set forth on pages 2-6.

Remarks begin on page 7.

AMENDMENT TO THE CLAIMS

Please **ADD** claim 31.

A copy of all pending claims and a status of the claims is provided below.

1. (original) A method for manufacturing a device including an n-type device and a p-type device, comprising:

forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device;

adjusting the shallow-trench-isolation oxide corresponding to at least one of the n-type device and the p-type device such that a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is different from a thickness of the shallow-trench-isolation oxide adjacent to the p-type device; and

forming a strain layer over the semiconductor substrate.

2. (original) The method of claim 1, wherein the strain layer comprises an etch stop nitride film.

3. (original) The method of claim 1, wherein the strain layer is one of a compressive strain layer or a tensile strain layer.

4. (original) The method of claim 1, wherein the step of adjusting comprises forming a pad nitride with a first thickness for the n-type device and forming a pad

nitride with a second thickness for the p-type device such that the first thickness is different from the second thickness.

5. (original) The method of claim 4, wherein the first thickness is smaller than the second thickness.

6. (original) The method of claim 4, wherein the first thickness is greater than the second thickness.

7. (original) The method of claim 1, wherein the step of adjusting comprises covering the n-type transistor while exposing the semiconductor substrate to at least one oxide etching chemical, such that a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is greater than the thickness of the shallow-trench-isolation oxide adjacent to the p-type device.

8. (original) The method of claim 7, wherein the oxide etching chemical includes HF (hydrofluoric acid).

9. (original) The method of claim 1, wherein the step of adjusting comprises covering the p-type transistor while exposing the n-type transistor and the semiconductor substrate to at least one oxide etching chemical, such that a thickness of the shallow-trench-isolation oxide adjacent to the p-type device is greater than the thickness of the shallow-trench-isolation oxide adjacent to the n-type device.

10. (original) The method of claim 9, wherein the oxide etching chemical includes HF.

11. (original) The method of claim 1, wherein the step of forming a strain layer comprises forming at least one of a SiGe, Si_3N_4, SiO_2 and Sio_xN_y layer on the semiconductor substrate.

12. (original) The method of claim 1, wherein the step of forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device comprises forming the shallow-trench-isolation oxide at a distance of about 1500 Angstroms or less from the adjacent n-type device or p-type device.

13. (original) The method of claim 1, wherein the thickness of the shallow-trench-isolation oxide of one of the n-type device or the p-type device is about 300 Angstroms to about 1000 Angstroms less than the shallow-trench-isolation oxide of the other of the n-type device or the p-type device.

14. (original) A method for manufacturing a device including an n-type device and a p-type device, comprising:

forming a boundary for the n-type device and the p-type device;

adjusting a height of the boundary such that a boundary adjacent to the n-type device is at a level which is different from a level of a height of a boundary adjacent to the p-type device; and

forming a strain layer over the semiconductor substrate.

15. (original) The method of claim 14, wherein the strain layer comprises a compressive strain layer or a tensile strain layer.

16. (original) The method of claim 15, wherein:

the strain layer is a tensile strain layer, and

the height of the boundary adjacent to the n-type device is lower than the height of the boundary adjacent to the p-type device.

17. (original) The method of claim 16, wherein:

the strain layer is a compressive strain layer, and

the height of the boundary adjacent to the p-type device is lower than the height of the boundary adjacent to the n-type device.

Claims 18-30. (canceled)

31. (new) A method for manufacturing a device including an n-type device and a p-type device, comprising:

forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device wherein a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is different from a thickness of the shallow-trench-isolation oxide adjacent to the p-type device; and

forming a strain layer over the semiconductor substrate.

REMARKS

Claims 1-17 and 31 are currently pending in the application. By this amendment, claim 31 is added for the Examiner's consideration. Applicants elect Group I, claims 1-17 and Species I, Figures 2A-2L, without traverse. Applicants provisionally elect claim 31, with traverse.

In the Notice of Non-Responsive Reply dated January 6, 2006, the Examiner acknowledged Applicants' earlier election filed October 26, 2005. The Examiner asserted that none of the claims indicated by the Applicants read on the elected species (Species I), noting the inclusion of the adjusting limitation. Applicants respectfully disagree and submit that claims 1-17 read on Species I.

In the Restriction Requirement dated September 28, 2005, the Examiner required restriction to one of two inventions defined as Group I, claims 1-17, drawn to a method, and Group II, claims 18-30, drawn to a device. The Examiner further stated that if either Group I or Group II was elected, then a further election of a single species would be required. The Examiner defined Species I as figures 2A-2L, Species II as figure 3, Species III as figure 4, and Species IV as figure 5.

Applicants appreciate the courtesies extended by Examiner Chen in the telephone conversation between the Examiner and Applicants' representative on February 2, 2006. Unfortunately, due to a USPTO computer problem, the issues presented in the Notice of Non-Responsive Reply could not be resolved over the telephone at that time. The Examiner is invited to contact the undersigned at the telephone number provided below, if necessary.

Applicants submit that Figure 2K is within the range defined as Species I (figures 2A-2L). Figure 2K is described in paragraph [0034] of the instant application, which states:

> [0034] After salicidation is completed, in the **methods according to this invention** an etch stop nitride film 245 is deposited over the wafer, as shown in **FIG. 2(k)**. The film

> may be of tensile stress or compressive stress. Depending on the topography of the shallow-trench-isolation oxide (STI) which surrounds and/or isolates one device from another device, the stress level induced in the transistor channel may be changed. Thus, by **adjusting the thickness of the shallow-trench-isolation oxide** which is adjacent to and/or isolates one device from the others, it is possible to adjust the stress level in the corresponding transistor channel such that the desired stress type (i.e., compressive or tensile) is formed therein.

It is clear from a fair reading of the above passage that the feature of adjusting the thickness of the shallow trench isolation oxide is described in reference to figure 2K, which is included in the range of figures 2A-2L. Independent claims 1 and 14 are both drawn to a method and contain the adjusting feature. Thus, claims 1-17 read on figures 2A-2L, and Applicants' election of October 26, 2005, is proper and fully responsive.

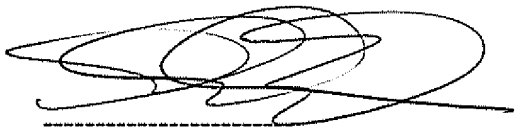
Applicants further submit that claims 1 and 14 are generic claims since the recitation of features by definition includes the features shown in figures 4 and 5. Applicants submit that claims 1-17 read on the elected species in addition to Figures 4 and 5.

In the event that the Examiner does not agree that claims 1-17 read on Species I and does not withdraw the Notice of Non-Responsive Reply, Applicants provisionally elect claim 31, with traverse. Applicants submit that new claim 31 reads on Group I because claim 31 is drawn to a method for manufacturing a semiconductor device without the adjusting step; albeit the thickness of the STI is recited as being different with respect to a p-type device and an n-type device. Applicants submit that new claim 31 reads on Species I, figures 2A-2L, because claim 31 does not contain the "adjusting" feature that was identified by the Examiner in the Notice of Non-Responsive Reply.

Accordingly, Applicants respectfully request that the Notice of Non-Responsive Reply be withdrawn and that claims 1-17 and 31 be examined on the merits.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0458.

Respectfully submitted,
Haining S. YANG



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